K.S ACADEMY, SALEM

PG TRB ,ENG & POLYTECHNIC TRB & TNSET

COACHING CENTRE FOR PHYSICS

POLYTECHNIC TRB STUDY MATERIAL

Unit 9: ELECTRONICS

****

Transistor.

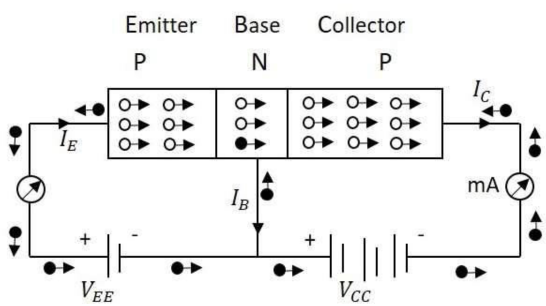
A **Transistor** is a three terminal semiconductor device that regulates current or voltage flow and acts as a switch or gate for signals.

- A transistor also acts as a **switch.**

Constraction:

The Transistor is a three terminal solid state device which is formed by connecting two diodes back to back. Hence it has **two PN junctions**. Three terminals are drawn out of the three semiconductor materials present in it. This type of connection offers two types of transistors. They are **PNP** and **NPN** which means an N-type material between two P types and the other is a P-type material between two N-types respectively.

The three terminals drawn from the transistor indicate Emitter, Base and Collector terminals.



Operation of a PNP transistor

Emitter

1. The left hand side of the above fig called as **Emitter**.
2. This has a **moderate size** and is **heavily doped** as its main function is to **supply**

a number of **majority carriers**, i.e. either electrons or holes.

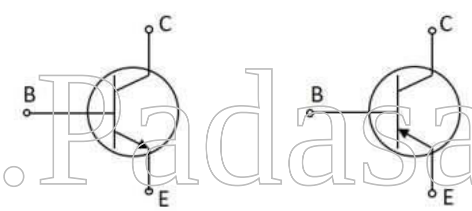
3. As this emits electrons, it is called as an Emitter.
4. This is simply indicated with the letter **E**.

Base

1. The middle material in the above figure is the **Base**.
2. This is **thin** and **lightly doped**.
3. Its main function is to **pass** the majority carriers from the emitter to the collector.
4. This is indicated by the letter **B**.

Collector

1. The right side material in the above fig called as a **Collector**.
2. Its name implies its function of **collecting the carriers**.
3. This is **a bit larger** in size than emitter and base. It is **moderately doped**.
4. This is indicated by the letter **C**.



Symbol of NPN transistor   Symbol of PNP transistor

The **arrow-head** in the above figures indicated the **emitter** of a transistor. As the collector of a transistor has to dissipate much greater power, it is made large. Due to the specific functions of emitter and collector, they are **not interchangeable**.

The **emitter base junction** is always **forward biased** as the emitter resistance is very small. The **collector base junction** is **reverse biased** and its resistance is higher. A small forward bias is sufficient at the emitter junction whereas a high reverse bias has to be applied at the collector junction.

The direction of current indicated in the circuits above, also called as the **Conventional Current**, is the movement of hole current which is **opposite to the electron current**.

Transistor biasing

The supply of suitable external dc voltage is called as **biasing**. Either forward or reverse biasing is done to the emitter and collector junctions of the transistor. These biasing methods make the transistor circuit to work in four kinds of regions such as **Active region**, **Saturation region**, **Cutoff region** and **Inverse active region** (not used).

EMITTER JUNCTION	**COLLECTOR JUNCTION**	**REGION OF OPERATION**
Forward biased	Forward biased	Saturation region
Forward biased	Reverse biased	Active region
Reverse biased	Forward biased	Inverse active region
Reverse biased	Reverse biased	Cut off region

Active region

This is the region in which transistors have many applications. This is also called as **linear region**. A transistor while in this region, acts better as an **Amplifier**. This region lies between saturation and cutoff. The transistor operates in active region when the emitter junction is forward biased and collector junction is reverse biased. In the active state, collector current is β times the base current, i.e.,

$$I_C = \beta I_B$$

Where

I_C = collector current

β = current amplification factor

I_B = base current

Saturation region

This is the region in which transistor tends to behave as a **closed switch**. The transistor has the effect of its collector and base being shorted. The collector and base currents are maximum in this mode of operation.

The transistor operates in saturation region when both the emitter and collector junctions are forward biased. As it is understood that, in the saturation region the transistor tends to behave as a closed switch, we can say that,

$I_C = I_E$

Where I_C = collector current and I_E = emitter current.

Cutoff region

This is the region in which transistor tends to behave as an **open switch**. The transistor has the effect of its collector and base being opened.

The transistor operates in cutoff region when both the emitter and collector junctions are reverse biased. As in cutoff region, the collector current, emitter current and base currents are nil, we can write as

$I_C = I_E = I_B = 0$

Where I_C = collector current, I_E = emitter current, and I_B = base current.

Bipolar Junction Transistor

A Bipolar junction transistor, shortly termed as **BJT** is called so as it has two PN junctions for its function. This BJT is nothing but a normal transistor. It has two types of configurations **NPN** and **PNP**. Usually NPN transistor is preferred

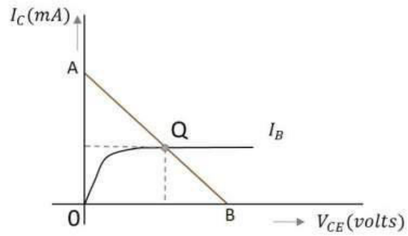
- ***BJT is a current controlled device.***

Operating point

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **saturation point**. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **cutoff point**.

When a line is drawn joining these two points, such a line can be called as **Load line**. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.

This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in active region.



The load line has to be drawn in order to obtain the Q-point. A transistor acts as a good amplifier when it is in active region and when it is made to operate at Q-point, faithful amplification is achieved.

Common emitter mode parameters:

Input impedance

It is defined as the ratio of small change in base- emitter voltage to the corresponding change in base current ***at constant*** V_{CE}

$$r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}}$$

Output impedance

It is defined as the ratio of small change in collector emitter voltage to the corresponding collector current ***at constant*** I_B

$$r_o = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$$

Crrent gain

It is defined as ratio small change in collector current to the corresponding change in base current **at constant** V_{CE}

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

Relation between α and β.

$\alpha -$ current gain in common base mode

$\beta -$ current gain in common emitter mode.

$$\alpha = \frac{I_c}{I_E}$$

$$\beta = \frac{I_c}{I_B}$$

$$\alpha = \frac{I_B}{I_B + I_c}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

β lies between 50 – 300

Early effect or base width modulation:

We know that in a PN junction the width of a depletion region increases as the reverse –bias voltage increases.

The emitter-base junction is unchanged because the voltage V_{be} is the same(emitter base junction is forward biased).

However the collector base junction is reverse biased . so a greater reverse bias across the collector–base junction, increases the collector–base depletion width . There is a lesser chance for recombination within the "smaller" base region. Since the is lightly doped as compared to the collector therefore the depletion region penetrates deeper into base region. This reduces width of the base region. **This variation or modulation of the effective base width by the collector voltage is known as Early effect or base width modulation**

Base punch through:

If reverse bias voltage of C-B junction is keep on increasing, a situation arises where E-B and C-B space charge regions touch each other, and the width of the base region becomes zero, Known as base punch through.

Field Effect Transistor:

An FET is a three-terminal unipolar semiconductor device. It is a **voltage controlled device** unlike a bipolar junction transistor(current controlled device). The main advantage of FET is that it has a very high input impedance, which is in the order of Mega Ohms. It has many advantages like low power consumption, low heat dissipation and FETs are highly efficient devices.

The FET is a **unipolar device**, which means that it is made using either p-type or n-type material as main substrate. Hence the current conduction of a FET is done by either electrons or holes.

Features of FET

- **Unipolar —** It is unipolar as either holes or electrons are responsible for conduction.

- **High input impedance —** The input current in a FET flows due to the reverse bias. Hence it has high input impedance.
- **Voltage controlled device —** As the output voltage of a FET is controlled by the gate input voltage, FET is called as the voltage controlled device.
- **Noise is low —** There are no junctions present in the conduction path. Hence noise is lower than in BJTs.
- **Gain is characterized as transconductance**. Transconductance is the ratio of change in output current to the change in input voltage.
- **The output impedance of a FET is low**.
- FET is used in circuits to reduce the loading effect.

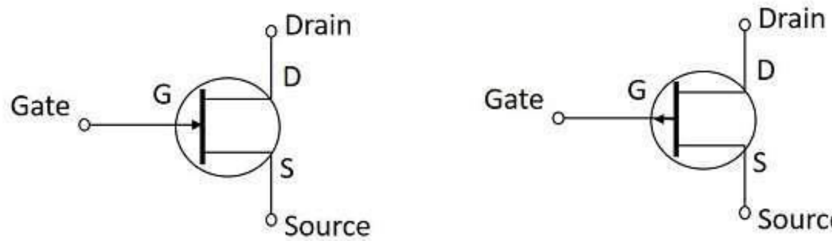
Advantages of FET

To prefer a FET over BJT, there should be few advantages of using FETs, rather than BJTs.

BJT	**JFET**
It is a bipolar device	It is an unipolar device
Current driven device	Voltage driven device
Low input impedance	High input impedance
Low thermal stability	High thermal stability
Gain is characterized by voltage gain	Gain is characterized by transconductance

Though FET is a three terminal device, they are not the same as BJT terminals. The three terminals of FET are Gate, Source and Drain. The **Source** terminal in FET is analogous to the Emitter in BJT, while **Gate** is analogous to Base and **Drain** to Collector.

The symbols of a FET for both NPN and PNP types are



Symbol of n-channel FET Symbol of p-channel FET

Source

- The Source terminal in a Field Effect Transistor is the one through which the carriers enter the channel.
- This is analogous to the emitter terminal in a Bipolar Junction Transistor.
- The Source terminal can be designated as **S**.
- The current entering the channel at Source terminal is indicated as $\mathbf{I_S}$.

Gate

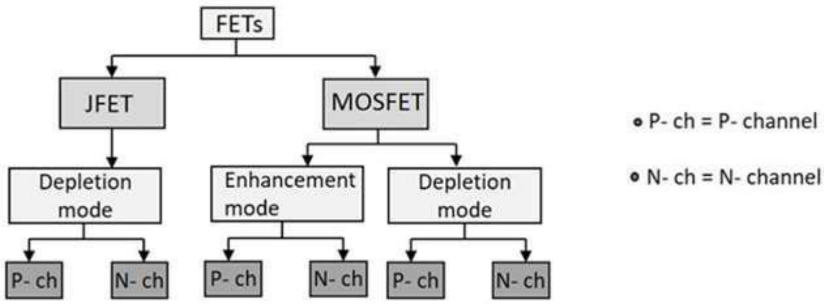
- The Gate terminal in a Field Effect Transistor **plays a key role in the function of FET** by controlling the current through the channel.
- By applying an external voltage at Gate terminal, the current through it can be controlled.
- Gate is a combination of two terminals connected internally that are heavily doped.
- The channel conductivity is said to be modulated by the Gate terminal.
- This is analogous to the base terminal in a Bipolar Junction Transistor.
- The Gate terminal can be designated as **G**.
- The current entering the channel at Gate terminal is indicated as $\mathbf{I_G}$.

Drain

- The Drain terminal in a Field Effect Transistor is the one through which the carriers leave the channel.
- This is analogous to the collector terminal in a Bipolar Junction Transistor.
- The Drain to Source voltage is designated as $\mathbf{V_{DS}}$.
- The Drain terminal can be designated as **D**.
- The current leaving the channel at Drain terminal is indicated as $\mathbf{I_D}$.

Types of FET

There are two main types of FETS. They are JFET and MOSFET. The following figure gives further classification of FETs.

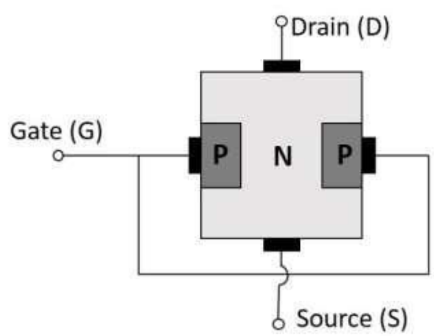


The JFET is abbreviated as **Junction Field Effect Transistor**. JFET is just like a normal FET. The types of JFET are n-channel FET and P-channel FET. A p-type material is added to the n-type substrate in n-channel FET, whereas an n-type material is added to the p-type substrate in p-channel FET.

N-Channel FET

The N-channel FET is the mostly used Field Effect Transistor. For the fabrication of N-channel FET, a narrow bar of N-type semiconductor is taken on which P-type material is formed by diffusion on the opposite sides. These two sides are joined to as gate terminal.

These two gate depositions (p-type materials) form two PN diodes. The area between gates is called as a **channel**. The majority carriers pass through this channel.



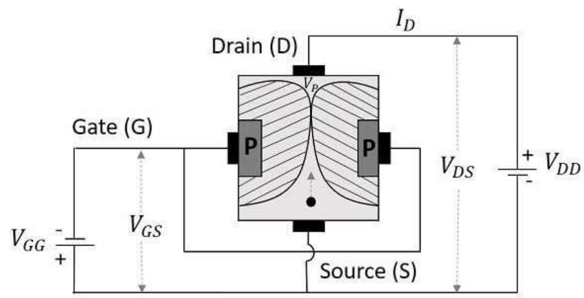
Structure of N-channel FET

Depletion Mode of Operation

As the **width of depletion layer plays an important role in the operation of FET**, the name depletion mode of operation implies. We have another mode called enhancement mode of operation, which will be discussed in the operation of MOSFETs. But **JFETs have only depletion mode** of operation.

Let us consider that there is no potential applied between gate and source terminals and a potential V_{DD} is applied between drain and source. Now, a current I_D flows from drain to source terminal, **at its maximum** as the channel width is more.

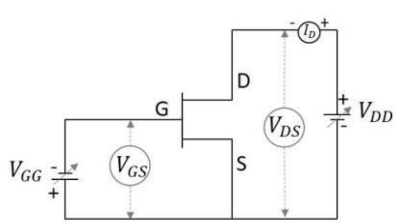
Let the voltage applied between gate and source terminal V_{GG} is reverse biased. This increases the depletion width. As the layers grow, the cross-section of the channel decreases and hence the drain current $(I_D)_{max}$ also decreases. .

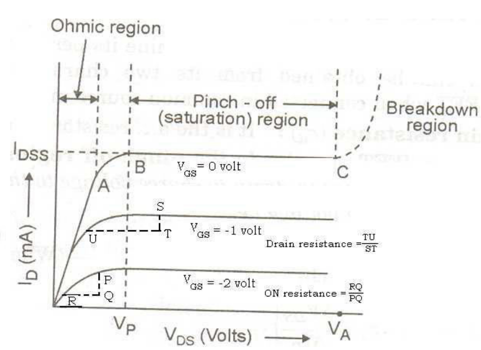


The voltage at which both these depletion layers literally "touch" is called as "**Pinch off voltage**". It is indicated as V_P. The drain current is literally nil at this point. Hence the drain current is a function of reverse bias voltage at gate.

Gate voltage controls the drain current, FET is called as the **voltage controlled device**.

Drain Characteristics of JFET:





1. I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that In normal operation of JFET.

2. There is a maximum drain voltage [V_{DS}(max)] that can be applied to a JFET. If the drain voltage exceeds V_{DS}(max), JFET would breakdown as shown in fig.
3. The region between V_P and V_{DS} (max) (breakdown voltage) is called constant-current region or active region. As long as V_{DS} is kept within this range, I_D will remain constant for a constant valueof V_{GS}. So we can say in the active region, JFET behaves as a constant–current device. For proper working of JFET, it must be operated in the active region.

Pinch off Voltage (V_P):

It is the minimum drain-source voltage at which the drain current essentially becomes constant. Gate-source cut off voltage V_{GS} (off). It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.

As gate-source cut off voltage [i.e V_{GS} (off)] on the transfer characteristic is equal to pinch off voltage V_P on the drain characteristic

$V_P = |V_{GS(Off)}|$

Expression for Drain Current is

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(Off)}}\right]^2$$

Where I_D = drain current at given VGS

I_{DSS} = shorted – gate drain current

V_{GS} = gate–source voltage

$V_{GS\ (off)}$ = gate–source cut off voltage

<u>JFET Parameters</u>

A.C drain resistance (r_d)

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage i.e.

A.C. drain resistance, $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}

Transconductance (g_{fs})

It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage

Transconductance $g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$ at constant V_{DS}

Amplification factor (μ)

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current.

Amplification factor, $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ at constant I_D

Note: amplification factor = a.c. drain resistance . transconductance

$$\mu = r_d \times g_{fs}$$

Gate to source resistance= $\frac{V_{GS}}{I_G}$

Features of JFET

1. A JFET is a three-terminal voltage-controlled semiconductor device i.e. input voltage controls the output characteristics of JFET.
2. The JFET is always operated with gate-source pn junction reverse biased.
3. In a JFET, the gate current is zero i.e. $I_G = 0A$.
4. Since there is no gate current, $I_D = I_S$.
5. The JFET must be operated between V_{GS} and V_{GS} (off). For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.
6. Because the two gates are at the same potential, both depletion layers widen or narrow down by an equal amount.
7. The JFET is not subjected to thermal runaway when the temperature of the device increases.
8. The drain current I_D is controlled by changing the channel width.

Drawbacks

FETs have a few disadvantages like high drain resistance, moderate input impedance and slower operation. To overcome these disadvantages, the MOSFET which is an advanced FET is invented. MOSFET stands for Metal Oxide Silicon Field Effect Transistor or Metal Oxide Semiconductor Field Effect Transistor. This is also called as **IGFET** meaning Insulated Gate Field Effect Transistor. The FET is operated in both depletion and enhancement modes of operation.

****

OBJECTIVE QUESTIONS

(I)Each question carries one mark

1. Which of the following statement is not true

1) JFET is a Voltage driven device

2) BJT is a It is a bipolar device

3) IGFET operated in both Enhancement and Depletion modes

4) FET operated in both Enhancement and Depletion modes

a) 1 & 3 b) 1 & 4 c) 4 only d) 3 only

2. The *early effect* in bipolar transistor is caused by

a) Decrease in junction temperature b) Large collector-base reverse-bias

c) Large emitter-base forward-bias d) Increase in junction temperature

3. A transistor in common emitter mode has

a) a high input resistance and low output resistance

b) a medium input resistance and high output resistance

c) a very low input resistance and a low output resistance

d) a high input resistance and a high output resistance

4. When gate source voltage is cutoff, then the JFET is said to be in

a) Saturated region

b) cut off region

c) negative resistance region

d) an open switch

5. In a *n*-channel *JFET*, the charge carriers are

a) electrons

b) holes

c) both electrons and holes

d) none of the above

6. Pinch-off voltage V_P for an FET is the drain voltage at which

a) significant drain current starts flowing

b) drain current becomes zero

c) all free charges get removed from the channel

d) avalanche break down takes place

7. Read the following statements and choose which one of the following is correct about operating point of a transistor

a) Operating point is the Values of I_C and V_{CE} when signal is applied to the transistor

b) Operating point is the Values of I_C and V_{CE} when Proper direct current is applied to the transistor

c) Operating point is the Values of I_C and V_{BE} when zero signal is applied to the transistor

d) Operating point is the Values of I_C and V_{CE} when zero signal is applied to the transistor

8. When a silicon transistor is properly biased, what is VBE for a C-E configuration?

a) voltage-divider bias

b) 0.3 V

c) 0.7 V

d) 0.5 V

9. Which of the following conditions are needed to properly bias an *npn* transistor amplifier?

a) Apply a large voltage on the base.

b) Forward bias the collector-base junction and reverse bias the emitter-base junction.

c) Apply a positive voltage on the *n*-type material and a negative voltage on the *p*-type material.

d) Forward bias the base-emitter junction and reverse bias the base-collector junction.

10. A *JFET* is a

a) unipolar device b) bipolar device

c) unijunction device d) both a & c

11. In an n-channel JFET, what will happen at the pinch-off voltage?

a) the value of V_{DS} at which further increases in VDS will cause no further increase in I_D

b) the value of V_{GS} at which further decreases in V_{GS} will cause no further increases in I_D

c) the value of V_{DG} at which further decreases in V_{DG} will cause no further increases in I_D

d) the value of V_{DS} at which further increases in V_{GS} will cause no further increases in I_D

(II)<u>Each question carries two marks</u>

12. A certain *JFET* data sheet gives $V_{GS(Off)} = -6V$ The pinch-off voltage V_P is

a) -5 V b) 3V C) 12V d) 6V

13. The reverse gate voltage of 15 V is applied to a JFET, the gate current is 10^3 μA. Then the resistance between gate and source is

a) $15 \times 10^4 \Omega$ b) $15 \times 10^9 \Omega$ c) $23 \times 10^4 \Omega$ d) $23 \times 10^9 \Omega$

14. The parameters for an n-Channel JFET are Maximum drain current I_{DSS} = 10mA, Pinch off voltage, Vp = - 4V then the drain current for zero gate source voltage is

a) 10 mA b) 5.6 mA c) 5 mA d) zero

15. In a common emitter transistor amplifier, the output resistance is 500 KΩ and the current gain β = 49. If the power gain of the amplifier is 5×10^6, the input resistance is

a)325 Ω b) 165 Ω c) 225 Ω d) 240 Ω

16. The current gain α of a transistor is 0.995. If the change in emitter current is 10 mA, the change in base current is

a) 50 μA b) 100 μA c) 500 μA d) 25 Ma

17. In a transistor common emitter mode gain is 100, then common base mode gain is

a) 99 b) 0.99 c) 1.0 d) 1.01

18. Identify which of the following is wrong

1) collector is larger in size than emitter and base and it is lightly doped

2) base is used to pass the majority carriers from the emitter to the collector

3) The transistor operates in saturation region when both the emitter and collector junctions are forward biased

4) *BJT is a voltage controlled device*

a) 2& 4 wrong *b) 1& 3 wrong* *c) 2& 4 wrong* *d) 1& 4 wrong*

Answer key

Q.NO	OPTION	Q.NO	OPTION
1	C	11	A
2	B	12	D
3	B	13	B
4	A	14	A
5	A	15	D
6	C	16	A
7	D	17	C
8	C	18	D
9	D	19	
10	A	20	